(a) identifying a group of one or more memory cells each having a stored charge over a first threshold and less than a second threshold; and

(b) programming each memory cell of the group of one or more memory cells until each of the memory cells of the group of one or more memory cells has a stored charge over the second threshold.

40. The method of claim 39 wherein the first threshold corresponds to an erased-cell reference level plus a guardband level.

41. The method of claim 37 wherein the identifying corresponds to identifying a memory cell having a charge above the erased-cell reference level plus a guardband level.--

REMARKS

These remarks are in response to the to the Official Action mailed on April 21, 2000, requiring the Applicant to specifically apply each limitation of element of the copied claims to the disclosure of the application. This is supplied for claim 37 below as part of the Request for Declaration of Interference, claims 35, 36, and 38 having been cancelled to better focus this request. Additionally, several new claims have been added. New claim 39 is similar to cancelled claim 35, but not as specific as to how the "subset" of claim 35 is determined, its steps (a) and (b) now made more similar to that of claim 37. New claim 40 is the same as cancelled claim 36, but dependent on new claim 39. New claim 41 is similar to claim 40, or cancelled claim 36, but dependent upon claim 37 and with its language made to conform with that of this underlying claim.

REQUEST FOR DECLARATION OF INTERFERENCE

It is respectfully requested that an interference be declared between the present application and patent 5,835,413 of Hurter et al., referred to below as the "'413 patent". Claim 37 of the present applications an exact copy claims 8 of the '413 patent and is suggested as the count for the interference, as follows:

Count 1

A method of improving data retention in a nonvolatile writeable memory having an erased-cell reference level and a programmed-cell reference level, the nonvolatile writeable memory having a plurality of memory cells, each of the memory cells being in an erased state when storing a charge below the erased-cell reference level, and each of the memory cells being in a programmed state when storing a charge above the programmed-cell reference level, the method comprising the steps of:

(a) identifying a memory cell having a charge above the erased-cell reference level and below the programmed-cell reference level; and

(b) programming the memory cell until the charge of the memory cell is above the programmed-cell reference level.

35 U.S.C. 135(b)

Claim 37 of the present application was added by Preliminary Amendment, simultaneously with the filing of the present application on November 9, 1999. This is less than one year after the ~~476~~ 413 patent was granted on November 10, 1998.

Effective Filing Date

As specified in the "Cross-Reference to Related Application" section added to the beginning of the present application by the Preliminary Amendment filed on November 9, 1999, the present application is entitled to an effective filing date of May 20, 1992, due to the benefit of:

U.S. Ser. No. 08/908,265, filed August 7, 1997,

U.S. Ser. No. 08/406,677, filed March 20, 1995, now patent no. 5,657,332,

U.S. Ser. No. 07/886,030, filed May 20, 1992.

The ~~476~~ 413 patent is shown to have a United States filing date of December 20, 1996. This is more than four years later than the May 20, 1992, effective filing date of the present application.

Therefore, it is requested that the interference be declared with the Applicants of the present application designated the senior party.

Claims Corresponding to the Proposed Count 1

The proposed count 1 is an exact copy of claim 8 of the `413 patent. Claim 10 of the `413 patent provides more detail by expanding step (a) of claim 8 into steps (a)-(c). Claim 1 also provides a more specific implementation in its steps (a) and (b) of step (a) of claim 8, combined with a less specific preamble and designation of the voltages.

Support for the Proposed Count 1 in the Present Application

Count 1	Present Application
A method of improving data retention in a nonvolatile writeable memory having an erased-cell reference level and a programmed-cell reference level, the nonvolatile writeable memory having a plurality of memory cells, each of the memory cells being in an erased state when storing a charge below the erased-cell reference level, and each of the memory cells being in a programmed state when storing a charge above the programmed-cell reference level, the method comprising the steps of:	Such a method is the subject of the "scrubbing" described in the Summary at p. 6, ln. 23 to p. 8, ln. 13 and in more detail beginning at p. 20, ln. 27. The described embodiments are all nonvolatile writeable memories, the reference levels are shown schematically in Fig. 10 with exemplary values given in Fig. 11, and their use described with respect to Figs. 7 and 8. The erased-cell reference level is V_E and the programmed-cell reference level V_{PV}. (Also see the comment below.)
(a) identifying a memory cell having a charge above the erased-cell reference level and below the programmed-cell reference level; and	This process is shown in Fig. 9 and described starting on p. 24, ln. 27. Steps 903 and 904 determine if $V>V_{SL}>V_E$, steps 901 and 902 determine if $V<V_{SH}<V_{PV}$, by the "No" path in both cases.

(b) programming the memory cell until the charge of the memory cell is above the programmed-cell reference level.

If the cell is so identified, it goes to step 905 of Fig. 9: "a rewrite operation will be preformed...steps of this program operation follows the procedure set forth in Fig. 8." (p. 25, lns. 19-22)

As shown in its Figure 10, the present application discloses several different voltage levels for use with a two-state cell. The levels of the `413 patent, as shown for example in its Figure 3, are less numerous and correspond to a degenerate version of those in the application, with V_{PV} $=V_{PRH}=V_{SH}$ for the PROGRAMMED REFERENCE LEVEL 50, with $V_{PRL}=V_E$ as the ERASED REFERENCE LEVEL 54, and the GUARDBAND 64 being between $V_{PRL}=V_E$ and V_{SL}. The left hand column above uses V_E as the erased-cell reference level, but could alternately use V_{PRL}, and uses V_{PV} as the programmed-cell reference level, but could alternately use V_{PRH} or V_{SH}. In either case, step (a) places V in the range $V_{SL}<V<V_{SH}$ and thus between the two reference levels for any of these choices.

`413 Patent Prosecution File History

A review of the file history of the `413 patent reveals that the material in the present application was not cited during the `413 patent application process.

Conclusion

A prompt declaration of the requested interference is respectfully requested. In the meantime, however, if the Examiner has any questions about this request, application or disclosure statements, a telephone call to the undersigned is invited.

Dated:

Respectfully submitted,

By: _____

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